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Olivier Rayssac

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PATENT DEPARTMENT  
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EXAMINER

TRINH, MICHAEL MANH

ART UNIT

PAPER NUMBER

2822

MAIL DATE

DELIVERY MODE

08/19/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/775,917	<b>Applicant(s)</b> RAYSSAC ET AL.	
	<b>Examiner</b> Michael Trinh	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5,8-14 and 16-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,8-14 and 16-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

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## DETAILED ACTION

\*\*\* This office action is in response to Applicants' Amendment filed May 05, 2008. Claims 1-5,8-14,16-24 are pending, in which claims 23-24 have been newly added.

\*\*\* The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### *Claim Rejections - 35 USC § 103*

1. Claims 19,23,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Tayanaka (6,107,213).

Re claim 19, Matsui teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28; Figs 17A-17C, col 28, line 55 to col 31) method of thinning a wafer made of semiconductor material, the wafer (118 in Fig 22) having first and second opposing faces, which comprises: providing at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) on the first face of the wafer; implanting atomic species through the second face and into the wafer to obtain a zone 120 of weakness at a predetermined depth therein (Fig 22, col 34, line 57 through col 35; col 28, lines 38-52; col 34, lines 25-55), the zone defining a first portion of the wafer extending from the zone to the first face and a remaining portion constituted by the remaining portion of the wafer; removing the remaining portion from the first portion along the zone of weakness to thin the wafer, with the electronic components or circuit (e.g. 115 in Fig 22) remaining on the first face (Figs 2C,3C,210-22); wherein it is not necessary to perform the last step of repeating the implanting and removing steps until the first portion has a reduced thickness for constituting a self-supported thin layer for the electronic component or circuit. Re claim 23, wherein the first portion (e.g. the first portion 117, as shown in Figures 22,17D) comprising a self-supported portion between the electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) and the zone of weakness, and the electronic component or circuit is supported on the self-supported portion during and after the removal. Re claim 24, wherein the electronic component or circuit(115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) has opposing first and second sides, with the second side being supported on the self-supported portion (e.g. the first portion 117, as shown in Figures 22,17D) during and after the removal.

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Re claims 19,23,24, Matsui lacks applying a stiffener to a second face prior to the removing step.

However, Tayanaka teaches (at Figs 3B-3C; col 15, lines 22-45) applying a stiffener 15/14 to both first and second faces of the wafer prior to removing the remaining portions, and then removing the stiffener and the remaining portion from the first portion.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a thin electronic device layer of Matsui by applying at least a stiffener to a second face of the wafer prior to removing the remaining portions and the stiffener from the first portion, as taught by Tayanaka. This is because of the desirability to facilitate the step of thinning of the wafer by removing the remaining portions, wherein the stiffeners cover and protect both second and first faces of the wafers during separation.

2. Claims 1-4,8-11,16-18,20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Tayanaka (6,107,213), as applied to claims 19,23,24 above, and further of Hanson et al(5,920,764).

Re claim 1, Matsui and Tayanaka teach method of thinning a wafer made of semiconductor material as applied to claim 19 above and repeated herein, wherein removing the remaining portion from the first portion along the zone of weakness to thin the wafer, with the electronic components or circuit (e.g. 115 in Fig 22) remaining supported on the first face (Figs 2C,3C,210-22), after splitting, to provide a new second face opposite the first face on the first portion. Re further claim 2, thinning the wafer by a mechanical polishing method is prior to the implanting of the atomic species (col 35, lines 21-28). Re claim 3, Matsui also teaches providing at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) on the first face of the wafer prior to the implanting of the atomic species. Re claim 4, wherein the remaining portion of the wafer is removed by applying a heat treatment (col 13, lines 60 through col 14). Re claim 8, wherein the stiffener is formed by deposition (col 12, lines 40-48), wherein the stiffener (Fig 2C; 6,8,5) is applied to the second face of the wafer 1 prior to removing the remaining portion by the application of a heat treatment (col 12, lines 40 through col 13; col 13, line 60 through col 14). Re claim 9, wherein the stiffener 5 comprises a layer of silicon oxide (col 12, lines 35-48; Fig 2C). Re claim 10, wherein the stiffener 8,5,6

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comprises a rigid plate (col 12, line 35 through col 13; col 25, lines 23-25). Re claim 11, wherein the rigid plate comprises a monocrystalline (col 13, lines 25-32) or polycrystalline silicon material (col 12, lines 40-48). Re claim 16, wherein the wafer comprises silicon (col 11, line 65 through col 12, line 8). Re claim 17, wherein the wafer comprises a silicon on insulator wafer (col 11, lines 60-65; col 35, lines 60-67; col 17, lines 29-50). Re claim 18, wherein the wafer comprises germanium, an alloy of silicon and germanium, silicon carbide (col 64, lines 49-56). Re further claims 20,21, as applied to claim 1 above and repeated herein, Matsui further also teaches removing the remaining portion as a self-supporting layer having a thickness of less than 35 micron from the first portion along the zone of weakness to thin the wafer (10 to several tens of microns at col 62, lines 1-8; 1-47; Fig 64D; 0.1 to 2 microns at col 15, lines 11-20). Re claim 22, wherein the zone of weakness defines the remaining portion extending therefrom to the second face (Figs 22,17).

Re claims 1,20, Matsui thus lacks repeating the implanting and removing steps until the first portion having a reduced thickness.

However, Hanson teaches (at Figs 4-5,3,1; col 4, lines 37-40; col 1, line 1 through col 2; col 4, line 6 through col 5) performing a Smart-Cut process by implanting hydrogen into the wafer to form a zone of weakness, and removing the portion to thinning the wafer, wherein, if required, the process of implantation, heating, and fracture can be repeated until the desired thickness are removed so as to retain a wafer having reduced thickness (col 4, lines 37-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thinning a wafer made of a semiconductor material of Matsui by repeating the implanting and removing steps until the desired thickness are removed first portion has a reduced thickness, if required and if necessary, the process of implantation, heating, and fracture can be repeated until the desired thickness are removed, as taught by Hanson. This is because of the desirability to thinning and reduce a wafer having a desired thickness so that a thin wafer and small semiconductor devices can be fabricated.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Tayanaka (6,107,213) and Hanson et al (5,920,764), as applied to claims 1-4,7-11,16-18,20-22 above, and further of Henley (6,291,314).

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The references including Matsui, Tayanaka, and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18,20-22 above.

Re claim 5, as described above, the references already teach removing the remaining portion of the wafer by heating, but lack blowing a jet of fluid adjacent the zone of weakness.

However, Henley teaches (at Fig 14; col 19, line 51 through col 21) removing the remaining portion by heating or blowing a jet of fluid adjacent the zone of weakness (col 20, 62 through col 21; col 20, lines 35-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to removing the remaining portion of the wafer of Matsui by heating or blowing a jet of fluid adjacent the zone of weakness, as taught by Henley, because these removing techniques are alternative and art recognized equivalent methods for removing a portion of the wafer in an effective and reliable manner.

4. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al (6,191,007) taken with Tayanaka (6,107,213) and Hanson et al (5,920,764), as applied to claims 1-4,7-11,16-18,20-22 above, and further of Aspar et al (6,020,252) and Sayyah (2002/0055237).

The references including Matsui, Tayanaka and Hanson teaches (at least in Figs 22; col 34, line 57 through col 35; Figs 1-23,34; cols 12-28) method of thinning a wafer made of semiconductor material as applied to claims 1-4,7-11,16-18,20-22 above.

As described above to claim 10, the references already teach applying a stiffener comprising a rigid plate 8,5,6 (Matsui, col 12, line 35 through col 13; col 25, lines 23-25), but lack to use a stiffener comprising a flexible film (claim 12) or an adhesive film (claim 13), a wax layer (re claim 14).

However, Aspar teaches (at col 6, lines 6-39; Figs 3-4) applying a stiffener 8 comprising a rigid or flexible support (re claim 12), wherein the stiffener comprises an adhesive film (claim 13, col 6, lines 12-18). Tayanaka also teaches forming the stiffener 14/15 comprising a flexible support 15 including an adhesive layer 14 (Figs 3B-3C; col 15, lines 23-40). Sayyah also teaches

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(at Figs 1c-1g; col 1, paragraphs 6,34-36) using a release stiffener layer comprising an adhesive or a wax layer (paragraph 0006).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove a portion of the wafer of the references including Matsui by applying a stiffener on the substrate, wherein applying a stiffener 8 comprising a rigid or flexible support, wherein the stiffener comprises an adhesive film (col 6, lines 12-18), as taught by Aspar and Tayanaka, wherein using an adhesive or a wax layer is further taught by Sayyah. This is because these stiffeners of rigid or flexible and adhesive or wax layers are alternative and art recognized equivalent materials that can be effectively used as a support and release layer during the step of removing a portion of the wafer.

***Response to Amendment***

5. Applicant's remarks filed May 05, 2008 have been fully considered but they are not persuasive, and in view of the new ground(s) of rejection.

Applicant remarked (at 5/5/2008 remark page 7, last two lines) that "...keeps the electronic component or circuit remaining on the original face of the original wafer, is not disclosed or suggested in Matsui".

In response, it is noted and found totally unconvincing. Again, the electronic component patterns 115 were formed on the first face (i.e. the electronic component patterns 115 were formed on the first face of the layer 114a of the wafer substrate; see Figs. 22, 17C-17D) and still remained on that first face of the remaining thin wafer after splitting (regardless of being transfer to another substrate). Again, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In *Re Self*, 213 USPQ 1,5 (CCPA 1982); In *Re Priest*, 199 USPQ 11,15 (CCPA 1978).

Applicant alleged (at 5/5/08 remark page 7) that in Matsui

Also, the base substrate (for example, the substrate 112 in FIGS. 17C and 17D) that is bonded to the original wafer...must be sufficiently thick to support the structure during the subsequent splitting as shown in the figures....

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In response, this is noted and found totally unconvincing. First, in the present application, a base stiffener 9 (as shown in Figures 18-20) and the base stiffener (as shown in Figures 16-17) applied to the faces of the original wafer also serve as “supporting substrates” during the subsequent splitting. Thus, in the present application as shown in Figures 18-20, the electronic component or circuit is also buried. In Matsui, Figure 22, the electronic component patterns 115 were still formed and remained on the main first face of the original wafer even though there was having a supporting substrate 112 formed thereon.

Applicant further alleged (at 5/5/08 remark page 8) that

It is noted that the main faces of a semiconductor wafer are much like those of a coin. Any submerged region well buried within the coin is not considered to be a face. Similarly, the pattern in Matsui after splitting is not on a face that was opposite from the face through which the ions were implanted in FIG. 22. It is buried well below the thick support layer....

In response, this is noted and found unconvincing. The main first face of the semiconductor substrate is still its first face although this main first face is buried or covered by another layer thereon. Applicant apparently alleges that the electronic component or circuit formed on the first face is exposed. However, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In *Re Self*, 213 USPQ 1,5 (CCPA 1982); In *Re Priest*, 199 USPQ 11,15 (CCPA 1978). In Matsui, in Figure 22, before splitting, the electronic component patterns 115 and 114b were formed on the main first face of the semiconductor wafer (i.e. the electronic patterns 115 were formed on the main first face of the layer 114a of the semiconductor substrate 114a/118), and the atomic species are implanted through the second bottom and opposite face of the semiconductor substrate 118. After splitting, the electronic component patterns 115 were still remained on the *same* main first face of the semiconductor wafer (i.e. the electronic patterns 115 were formed on the first face of the layer 114a of the semiconductor substrate 114a/118) even though there was having a supporting substrate 112 formed thereon.

Applying a stiffener as taught by Tayanaka would have been obvious because at least of the desirability to facilitate the removal or cleaving of the weak zone. Herein, Tayanaka clearly teaches (at Figs 3B-3C; col 15, lines 22-45) applying a stiffener 15/14 to both first and second faces of the wafer prior to removing the remaining portions, and removing the stiffener and the



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remaining portion from the first portion. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971); In re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In re Simon, 174 USPQ 114 (CCPA 1972); In re Richman 165 USPQ 509, 514 (CCPA 1970).

Matsui clearly teaches the claimed invention by removing the remaining portion of the wafer to reduced its wafer thickness so as to provide a self-supporting thin wafer with a thickness of less than 35 micron from the first portion along the zone of weakness, wherein the thinning wafer after reducing its thickness has a reduced thickness of about 10 microns to several tens of microns (see column 62, lines 1-8; 1-47; Fig 64D; with 0.1 to 2 microns at col 15, lines 11-20 (“several” is defined as being more than two or three but not many). This thinner wafer after thinning and reducing its thickness together with circuit layers on its first face is constituting a self-supported thin layer for the electronic component circuit formed thereon.

Applicant's remarks about Hanson are noted and found unconvincing. Hanson et al reference teaches repeating the Smart-Cut process by implanting hydrogen into the wafer to form a zone of weakness at a certain depth (about 5000 Angstroms to 3  $\mu\text{m}$ ), and removing the portion to thinning the wafer, wherein, if required, the process of implantation, heating, and fracture can be repeated until the desired thickness are removed so as to retain a wafer having reduced thickness (col 4, lines 37-40; Figs 4-5,3,1; col 4, lines 37-40; col 1, line 1 through col 2; col 4, line 6 through col 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to thinning a wafer made of a semiconductor material of Matsui by repeating the thinning process until the desired thickness are obtained, as taught by Hanson, if required and if necessary. This is because of the desirability to thinning and to reduce the wafer thickness until the desired thickness are obtained so that thinner and smaller semiconductor devices can be fabricated. The primary reference of Matsui clearly teaches forming at least one electronic component or circuit (115 in Fig 22; 225/223 in Fig 34; 2,3 in Figs 1-4; col 12, lines 1-35) on the first face of the wafer. In Matsui, the semiconductor wafer is having a thickness of about a few hundred micrometers (col 35, lines 12-28); and thus, in view of Hanson, repeating the implanting and removing step would have been obvious to one of ordinary

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skill in the art in order to reduce the thickness of the wafer to have a desired thickness, wherein just after the first splitting and removing step, the first portion the wafer having a reduced thickness also constitutes a self-supported thin layer for the electronic component or circuit supported on the first face. Thus, the rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In *Re Lyons* 150 USPQ 741 (CCPA 1966). Moreover, it is well settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In *Re Keller*, 208 USPQ 871 (CCPA 1981); In *Re Young*, 159 USPQ 725 (CCPA 1968).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).  
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/Michael Trinh/  
Primary Examiner, Art Unit 2822